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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/031,672	09/09/2002	William C. Athas	18036-24199	6837

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EXAMINER	
CHO, JAMES HYONCHOL	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 01/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/031,672	ATHAS ET AL.	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-29* is/are allowed.

6)☒ Claim(s) *30 and 32-41* is/are rejected.

7)☒ Claim(s) *31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 8, 2004 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 30, 35 and 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Sigal (US PAT No. 5,504,441).

Regarding claim 30, Figs. 1, 2, 3A and 3B of Sigal teaches a clock-powered logic system (logics are enabled, i.e. empowered and controlled by clocks) containing logic (Fig. 3A) configured to be connected to a supply voltage (see Fig. 1) and configured to be powered by a set of substantially complementary and substantially non-overlapping clocks (CLOCK1 and CLOCK2 in Fig. 3B; dynamic logic gates controlled by CLOCK1 and CLOCK2) having a voltage of a magnitude that does not exceed the magnitude of the supply voltage (col. 1, line 43+).

Regarding claim 35, Figs. 1, 2, 3A and 3B of Sigal teaches the clock-powered logic system of claim 30 where the system includes an n-latch (Fig. 2 latch comprising N20, N21, P20, P21, I20-I22).

Regarding claim 37, Figs. 1, 2, 3A and 3B of Sigal teaches the clock-powered logic system of claim 30 where the system includes a clocked buffer (dynamic logic gate comprising P10, P14, N10-14 in Fig. 1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 32-34 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sigal (US PAT No. 5,504,441) in view of Han (UK GB 2,248,988).

Regarding claims 32-34 and 36, Figs. 1, 2, 3A and 3B of Sigal discloses the clock-powered logic system of claim 30, but does not disclose the system including a jam latch, a signal level booster, a pulse-to-level converter, or a device that can be clocked by a signal of smaller magnitude than the supply voltage.

However, Fig. 3 of Han discloses a signal level booster, a jam latch, or a pulse-to-level converter having an input and an output having a greater magnitude for the purpose of providing double voltage source interface circuit with reduced power consumption.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use a jam latch, a signal level booster, or a pulse-to-level converter of Han in the system of Sigal because it would provide an interface circuit with a reduced power consumption.

Claims 38-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sigal (US PAT No. 5,504,441) in view of Dickinson (US PAT No. 5,521,538).

Regarding claims 38-41, Figs. 1, 2, 3A and 3B of Sigal discloses the clock-powered logic system of claim 30, but does not disclose the system is configured to utilize an adiabatic signal including blips or a ramp signal, or a staircase signal. However, Fig. 1 of Dickinson teaches an adiabatic logic circuit having the same switching potential as a CMOS logic and the adiabatic logic provides low-power consumption (col. 1, lines 16-63). Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to use an adiabatic signal including blips or a ramp signal, or a staircase signal as an input signal of Dickinson for the purpose of providing compatibility among different data signals.

Allowable Subject Matter

Claims 1-29 are allowable over the prior art of record.

Claim 31 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed November 8, 2004 have been fully considered but they are not persuasive regarding claims 30, 32-41.

On pages 2-3 of the amendment, applicant argues that Figs. 1, 2, 3A and 3B of Sigal does not teach clock-powered logic specified in the first line of claim 30. However, the examiner notes that Figs. 1, 2, 3A and 3B of Sigal DOES teach the logic system enabled, i.e. empowered and controlled by clock signals, CLOCK1 and CLOCK2. The examiner further notes that the first line of claim 30 which recites "A clock-powered logic system containing logic" DOES NOT have any bearing on the applicant's statement of "The output of a logic stage comprises a clock signal controlled by the input to that stage". In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the source of the OUTPUT signal being derived from a gated clock signal) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The examiner further notes that the recitation "Clock-powered logic" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended

use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).). Therefore, Figs. 1, 2, 3A and 3B of Sigal teaches all claimed limitations.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H. Cho
Primary Examiner
Art Unit 2819

January 18, 2005